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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,765	12/24/2003	Hideaki Nagasawa	402924	9452

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,765	NAGASAWA ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/743,765 filed 12/24/2003.

2. Claims 1-18 are pending in the Application.

Claim Objections

3. Claims 4, 5, 7, 9, 13, 14 16, 18 are objected to because of the following informalities:

claim 4 line 4 after "described" delete "," insert --;--

claim 5 line 5 after "described" delete "," insert --;--

claim 7 line 5 after "connections" delete "," insert --;--

claim 9 line 9 after "described" delete "," insert --;--

claim 13 line 6 after "described" delete "," insert --;--

claim 14 line 5 after "described" delete "," insert --;--

claim 16 line 5 after "connections" delete "," insert --;--

claim 18 line 9 after "described" delete "," insert --;--

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6, 9-15 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Watkins et al. (US Patent 5,867,395).

With respect to claims 1 and 10 Watkins et al. teaches an automatic circuit design apparatus within method for reverse-synthesize gate netlist level definitions into RTL definition of an integrated circuit design (abstract; col. 2, ll.29-32), a computer-implemented automatic circuit design method by computer program executable or apparatus to process netlist definitions to produce RTL design (col. 2, ll.60-63), comprising: an analyzer for analyzing a data set in a form of a table within identifying all the netlist patterns (data set) as a part of the analyzing process as a step 22 of the Fig. 2 (col. 3, ll.40-42), wherein the information obtained during the parsing and analyzing of the netlist may be saved as a table (col. 3, ll.24-26), both connection conditions concerning a plurality of circuit components within an integrated circuit and connections among the circuit components in each of the connection conditions being described in the data set within tracing each input and output of the identified pattern to its termination point as a primary input and output as well as input and output connections of the another identified pattern (col. 3, ll.43-53); and a description creating unit for creating a description of the integrated circuit with a hardware description language based on analytical results from the analyzer within a step 30 of the Fig. 2, wherein generation of the RTL design is automatically processed with utilizing the information of all identified patterns in the netlist, which correlate with RTL constructs (col. 3, ll.55-62).

With respect to claims 2-6, 9, 11-15 and 18 Watkins et al teaches:

Claims 2, 11: description creating unit selects one or more selector modules suitable for implementing connections among the plurality of circuit components in each of the connection conditions based on the analytical results from the analyzer, and adds information about the one or more selector modules to the description of the integrated circuit within a step 80 as shown on the Fig. 5A for selecting module under test (MUT) from the RTL description (col. 5, ll.40-42) to correlate inputs and outputs of the components in selected module and the connections between components with the same MUT determined in the netlist (analytical results) as shown in the step 83, 84 of the Fig. 5A (col. 5, ll.49-54) and automatically finishes creation of the RTL description of the IC (col. 6, ll.42-46);

Claims 3, 12: description creating unit adds information about a control signal creating module suitable for creating a control signal used to control the one or more selector modules to the description of the integrated circuit based on the analytical results from the analyzer within generating automatically a test bench (control signal) to verify the correlation between identified module (MUT) in the RTL description with the corresponding module in the information obtained from analysis of the netlist of the same IC (col. 5, ll.49-54);

Claims 4, 13: the analyzer analyzes the data set in which the connection conditions including a normal use mode in which the integrated circuit normally operates and a plurality of secondary modes in which the integrated circuit secondarily operates are described within the process of analyzing the netlist includes generating of the hash table pointing to the input linked-lists containing information regarding the input and

output connections of each identified pattern from the netlist (col. 4, ll.18-20); and the description creating unit selects a first selector module disposed among the circuit components that are connected to one another in the normal use mode based on the analytical results from the analyzer, selects a second selector module suitable for implementing connections among the circuit components in each of the plurality of secondary modes, and adds information about the first and second selector modules to the description of the integrated circuit so that an output of the second selector module is connected to an input of the first selector module within steps 83 and 84 of the Fig. 5A, wherein selecting module under test from RTL description is processed to monitor the outputs of MUT (col. 5, ll.50-53) including primary input and output of the identified pattern (selected module) from netlist (analytical information) and information relating to the combination logic gates in between the identified pattern and the termination points of the input an output connections (col. 3, ll.45-52);

Claims 5, 13: the analyzer analyzes the data set in which the connection conditions including a normal use mode in which the integrated circuit normally operates and a secondary mode in which the integrated circuit secondarily operates are described within analyzing the netlist including tracing primary input and primary output of the identified pattern from netlist and information relating to the combination logic gates in between the identified pattern and the termination points of the input an output connections (col. 3, ll.45-52); and the description creating unit selects a gate module that effectively transmits a signal in the secondary mode among the circuit components that are connected to one another in the secondary mode based on the analytical

results from the analyzer and adds information about the gate module to the description of the integrated circuit within steps 83 and 84 of the Fig. 5A, wherein selecting module under test from RTL description is processed to monitor the outputs of MUT (col. 5, ll.50-53) including **primary** input and output of the identified pattern (selected module) from netlist (analytical information) and information relating to the combination logic gates in between the identified pattern and the termination points of the input an output connections (col. 3, ll.45-52)

Claims 6, 15: selected gate module has an output that is disabled in response to a control signal in the normal use mode as shown on the Figs. 3 and 4 illustrating implementation of the parse and the analysis process of the netlist including the element 61' containing the primary inputs as well as the combinational logic between the primary inputs and the connection 61 (col. 4, ll.18-20; ll.22-24; ll.35-37);

Claims 9, 18: the analyzer analyzes both a higher-level data set in a form of a table, in which both connection conditions concerning the plurality of circuit components within the integrated circuit and connections among the circuit components corresponding to each of the connection conditions are described, and a plurality of lower-level data sets in a form of a table, in each of which both connection conditions concerning internal elements within a corresponding one of the plurality of circuit components and connections among the internal elements corresponding to each of the connection conditions are described within hash table depicted on the Fig. 4, which collects the information gathers from parsing and analyzing of the netlist (higher level data set), as well as associated linked-lists (lower-level data set) (col. 3, ll.64-67; col. 4,

ll.16-20); and the description creating unit creates an overall description of the entire integrated circuit and the plurality of circuit components at a time based on the analytical results from the analyzer within the system for generating a RTL definition for IC design (col. 2, ll.29-31), wherein the RTL description is generated based on the analytical information of the netlist of the same IC (col. 3, ll.55-62).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7, 8, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins et al.

With respect to claims 7, 8, 16 and 17 Watkins et al. teaches the limitations from which the claims depend. Watkins et al. teaches the system for generating a RTL definition for an integrated circuit (IC) design by analyzing the netlist definition of the IC (col. 2, ll.29-32), including parsing and analyzing process of the netlist with tracing each input and output connections of all identified patterns in the netlist (col. 3, ll.45-50), wherein tracing the inputs and the outputs of the identified patterns, the information relating to the combination logic gates in between the identified pattern and the termination points of the input and the output connections is saved (col. 3, ll.48-52). However Watkins et al. lacks the specifics regarding feeding a power to each of the plurality of circuit components. It would have been obvious to one of ordinary skill in the

art at the time the invention was made that saved detailed information about each input and output connections for each component in the identified patterns from the netlist of the IC design including tracing to its termination point (which may be a primary input, a primary output of another identified pattern) might be used for determination and calculation of the power consumption (including information whether feeding of power to each of plurality of circuit components can be stopped) in the IC design (col. 3, ll.45-49).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

STACY A. WHITMORE
PRIMARY EXAMINER

Examiner
Helen Rossoshek
AU 2825